Claim 1 stands rejected under 35 U.S.C. 102(e) as being anticipated by Lee, et al. (U.S. Patent No. 6,232,651). Applicant respectfully traverses the rejection. Claim 1, as amended, includes the feature of "gold selectively plated on segments of said leadframe intended for solder attachment." Lee (col. 2, lines 25-38) teaches that "a gold thin layer can be formed on part of the external leads to protect the outermost palladium layer." However, Lee notes that use of a thin gold layer increases production costs and provides "bad" adhesiveness to mold resin. These statements in Lee are clear indications that Lee is not selectively plating gold on segments of the leadframe intended for solder attachment (why else would Lee worry about adhesiveness of gold to mold compound?), but is rather the plating of gold extensively over the external leads, and is therefore teaching away from the claimed invention. Moreover, Lee also notes that the gold layer reduces wetting time by expediting smooth dissolution of palladium and lead, but that the thin gold layer forms Au-Sn, thereby degrading solderability. Lee, therefore, teaches away from its use in enhancing solderability. For at least these reasons, Applicant respectfully submits that Claim 1 is patentable over Lee.

Claim 1 stands rejected under 35 U.S.C. 102(b) as being anticipated by Hashizume (U.S. Patent No. 5,946,556). Applicant respectfully traverses the rejection. As noted above, Claim 1 includes the feature of "gold selectively plated on segments of said leadframe intended for solder attachment." Hashizume (col. 10, lines 26-34) merely states that surfaces of a die pad and lead fingers are plated with a metal such as gold (Au) or silver (Ag). Hashizume does not state whether the entire leadframe is covered with the gold or silver layer, but it is clear that the gold or silver is not selective to segments of the leadframe intended for solder attachment. Therefore, Applicant respectfully submits that Claim 1 is patentable over Hashizume.

Claims 2 to 13 and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Abbott (U.S. Patent No. 6,245,448) in view of Akino, et al.

(Japan Patent Application #2000-77593) and further in view of Lee et al. (U.S. Patent No. 6,232,651). Claim 2, as amended, includes the feature of "gold selectively plated on segments of said leadframe intended for solder attachment." Abbott does not teach or suggest such a feature. Similarly, although Akino teaches the gold flash plating of the entire surface of the lead frame, such a teaching is merely cumulative to the art acknowledge in Applicant's specification (page 3, lines 18-19). As indicated above, Lee does not teach or suggest the claimed feature, but instead actually teaches away from the selective use of gold on leadframe segments intended for solder attachment. Therefore, Applicant submits that Claim 2 is patentable over the combined references since that combination does not teach or suggest all of the claimed features of the invention. Claims 3-9 depend from Claim 2 and are therefore patentable over the combined references for at least the reasons presented above. Claim 10 depends from Claim 1, which includes the same feature as cited above in Claim 2. Therefore, Claim 1 and Claim 10, which depends therefrom, are patentable over the combined references. Similarly, Claim 11 includes the same feature as cited above in Claim 2. Therefore, Applicant submits that Claim 11, and Claims 12 and 13 which depend therefrom, are patentable over the combined references for at least the reasons presented above.

Claims 2 to 13 and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Abbott in view of Akino in view of Hashizume. Claims 1, 2 and 11, as amended, include the feature of "gold selectively plated on segments of said leadframe intended for solder attachment." Abbott does not teach or suggest such a feature. Similarly, although Akino teaches the gold flash plating of the entire surface of the lead frame, such a teaching is merely cumulative to the art acknowledge in Applicant's specification (page 3, lines 18-19). As indicated above, Hashizume does not teach or suggest the selective plating of gold on leadframe segments intended for solder attachment. Since the combined references do not teach or suggest all of the claimed features,

Applicant submits that Claims 1, 2 and 11, as well as Claims 3-13 and 15 depending therefrom, are patentable over the combined references.

The Office Action contains the statement that, with respect to Claims 3 to 8, that the specification "contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom." Applicant disagrees. The importance of decreasing the thickness of the palladium layer is clearly indicated on page 11 of the instant specification (see the third paragraph on that page). In addition, the specification makes clear the significance of the relative thicknesses of the nickel (ductility), palladium (wire bonding and mold compound adhesion), and gold (prevent oxidation of the palladium as a result of soldering).

New Claim 23 includes the feature "gold selectively plated on portions of said lead segments intended for solder attachment" included in Claims 1, 2, and 11. Therefore, Applicant submits that it is patentable over the cited references. New Claims 24-26 feature the relative thicknesses of the palladium and nickel layers, support for which can be found on page 11 of the specification as indicated above. Applicant respectfully requests consideration and examination of these new claims.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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OIPE JC87
SEP 27 2002
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (amended) A leadframe for use with packaged integrated circuit chips comprising:

gold selectively plated on segments of said leadframe intended for solder attachment

[a plated layer of gold selectively covering segments of said leadframe external to said package, intended for solder attachment].

2. (amended) A leadframe for use with packaged integrated circuit chips, having a chip mount pad and a plurality of lead segments, comprising:

a leadframe base made of copper or copper alloy;

a first layer of nickel deposited on said copper or copper alloy;

a layer of an alloy of nickel and palladium on said first nickel layer;

a second layer of nickel on said alloy layer, said second nickel layer deposited to be suitable for bending of said lead segments, wire bonding, and solder attachment;

a layer of palladium, said palladium layer deposited to be suitable for protecting the nickel surface for wire bonding and solderability, and for adhesion to molding compound; and

gold selectively plated on segments of said leadframe intended for solder attachment

[a layer of gold selectively covering portions of said lead segments external to said package, intended for solder attachment].

11. (amended) A packaged semiconductor device comprising:

a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments having their first end near said mount pad and their second end remote from said mount pad;

said leadframe having a first surface layer of nickel, a layer of an alloy of nickel and palladium, a second layer of nickel, and a layer of palladium;

said leadframe further having gold selectively plated on segments of said leadframe intended for solder attachment [an outermost layer of gold selectively covering portions of said second ends of said lead segments external to said package, in a thickness suitable to optimize solder attachment];

an integrated circuit chip attached to said mount pad; and

bonding wires interconnecting said chip and said first ends of said lead segments.

14. (cancelled)

16. (cancelled)

17. (cancelled)

18. (cancelled)

19. (cancelled)

20. (cancelled)

21. (cancelled)

22. (cancelled)

Please add the following new claims:

23. (new) A packaged semiconductor device, comprising:

a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments;

said leadframe having a layer of nickel and a layer of palladium covering said chip mount pad and said plurality of lead segments, and gold selectively plated on portions of said lead segments intended for solder attachment;

an integrated circuit chip attached to said mount pad; and

bonding wires interconnecting said chip and said first ends of said lead segments.

24. (new) A packaged semiconductor device, comprising:

a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments;

said leadframe having a layer of nickel and a layer of palladium covering said chip mount pad and said plurality of lead segments, and gold selectively plated on portions of said lead segments intended for solder attachment, wherein said layer of palladium has a thickness in the range of about 0.03% to about 6% of a thickness of said nickel layer;

an integrated circuit chip attached to said mount pad; and

bonding wires interconnecting said chip and said first ends of said lead segments.

25. (new) The packaged semiconductor device, wherein said layer of nickel has a thickness in the range of about 500 nm to about 3000 nm and said palladium layer has a thickness in the range of about 10 nm to about 30 nm.

26. (new) The packaged semiconductor device, wherein said gold has a thickness in the range of about 6% to about 50% of said thickness of said palladium layer.